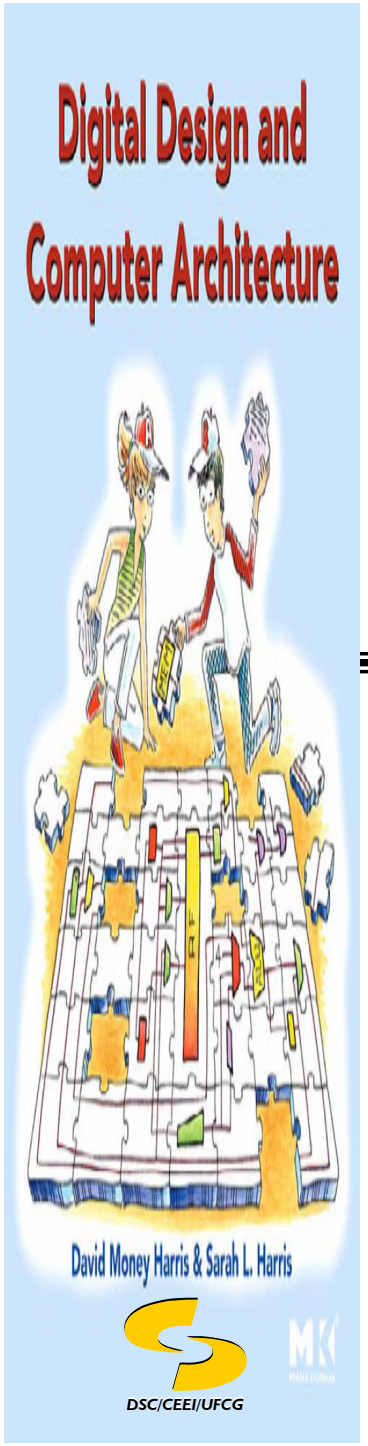


Universidade Federal de Campina Grande

Unidade Acadêmica de Sistemas e Computação

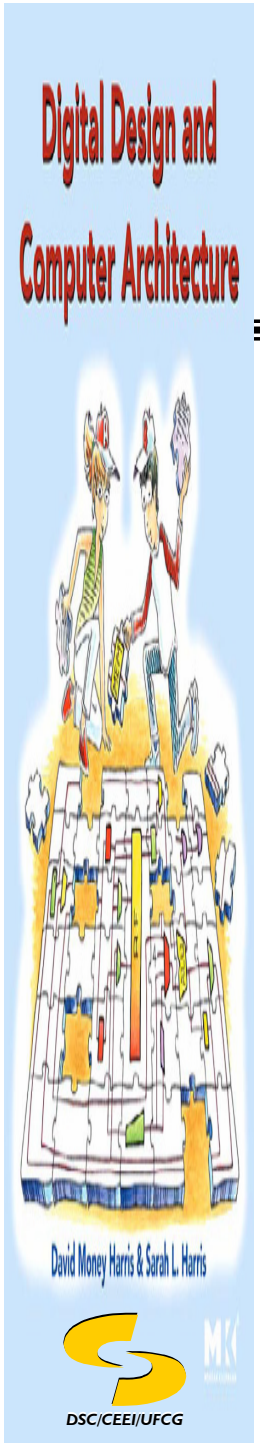
Curso de Bacharelado em Ciência da Computação

Organização e Arquitetura de Computadores I

Nível da Microarquitetura (Parte Complementar)

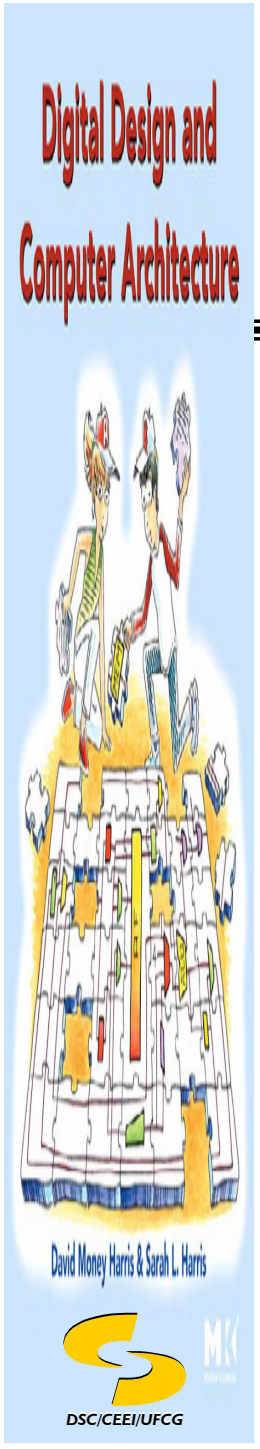
Profª Joseana Macêdo Fechine Régis de Araújo
joseana@computacao.ufcg.edu.br

Carga Horária: 60 horas



Tópicos

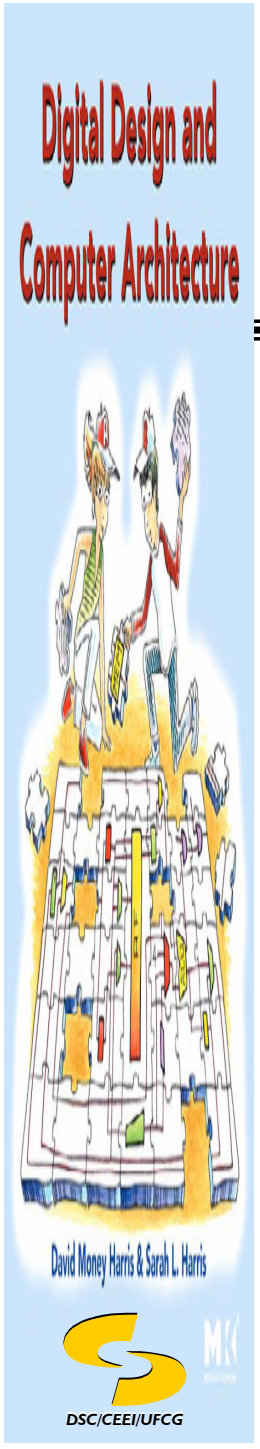
- Nível ISA
  - Nível da Microarquitetura
    - *Datapath*
    - Unidade de Controle



Microarquitetura

- **Microarquitetura**: forma como está implementada a arquitetura em hardware
- **Processador**:
  - *Datapath*: blocos funcionais
  - Controle: sinais de controle

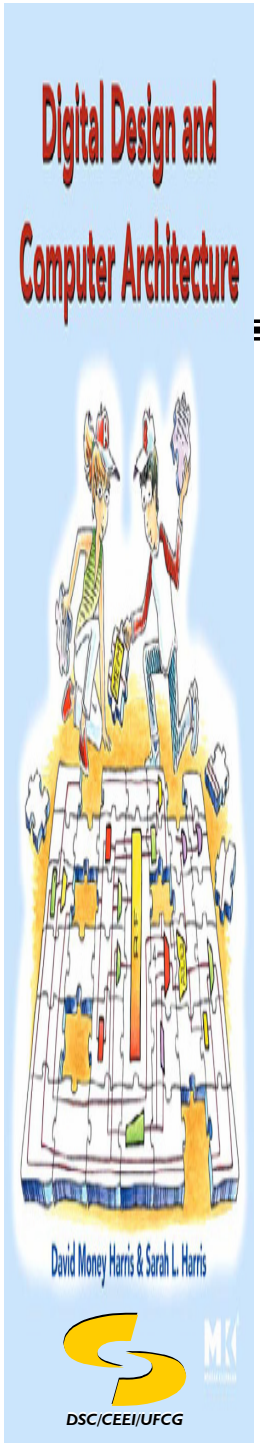
Application Software	programs
Operating Systems	device drivers
Architecture	instructions registers
Micro-architecture	datapaths controllers
Logic	adders memories
Digital Circuits	AND gates NOT gates
Analog Circuits	amplifiers filters
Devices	transistors diodes
Physics	electrons



Microarquitetura

Múltiplas implementações para uma mesma arquitetura:

- ***Single-cycle***
  - Cada instrução é executada em um único ciclo
- ***Multicycle***
  - A execução de cada instrução é dividida em uma série de passos menores
- ***Pipelined***
  - A execução de cada instrução é dividida em uma série de passos menores
  - Múltiplas instruções (parte de) executando ao mesmo tempo.



Microarquitetura

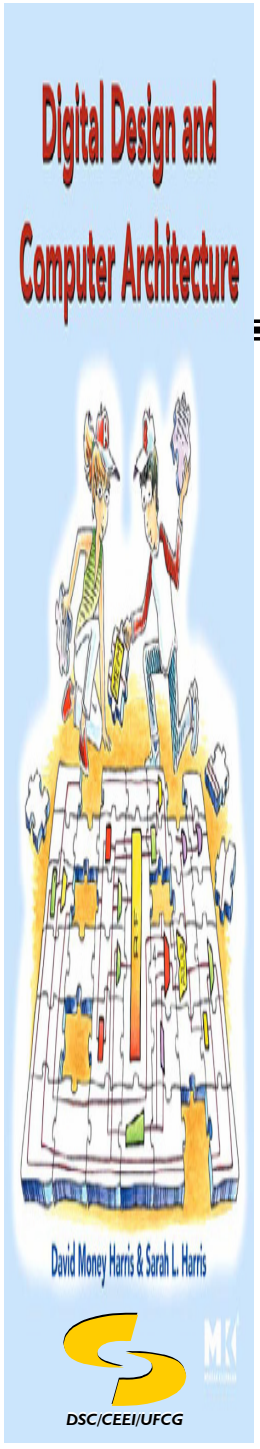
Conceitos importantes:

- ***Program execution time***

  Execution Time = (# instructions)(cycles/instruction)(seconds/cycle)

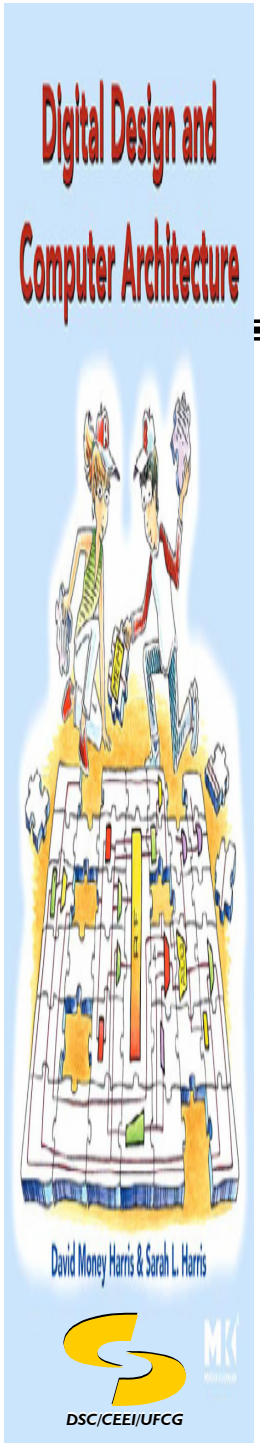
  - Cycles/instruction = CPI
  - Seconds/cycle = clock period
  - 1/CPI = Instructions/cycle = IPC

- **Desafios na implementação de uma microarquitetura**
  - **Custo**
  - ***Power***
  - **Desempenho**



Microarquitetura

- **Processador MIPS**
  - Subconjunto das instruções MIPS:
    - R-type instructions: `and`, `or`, `add`, `sub`, `slt`
    - Memory instructions: `lw`, `sw`
    - Branch instructions: `beq`

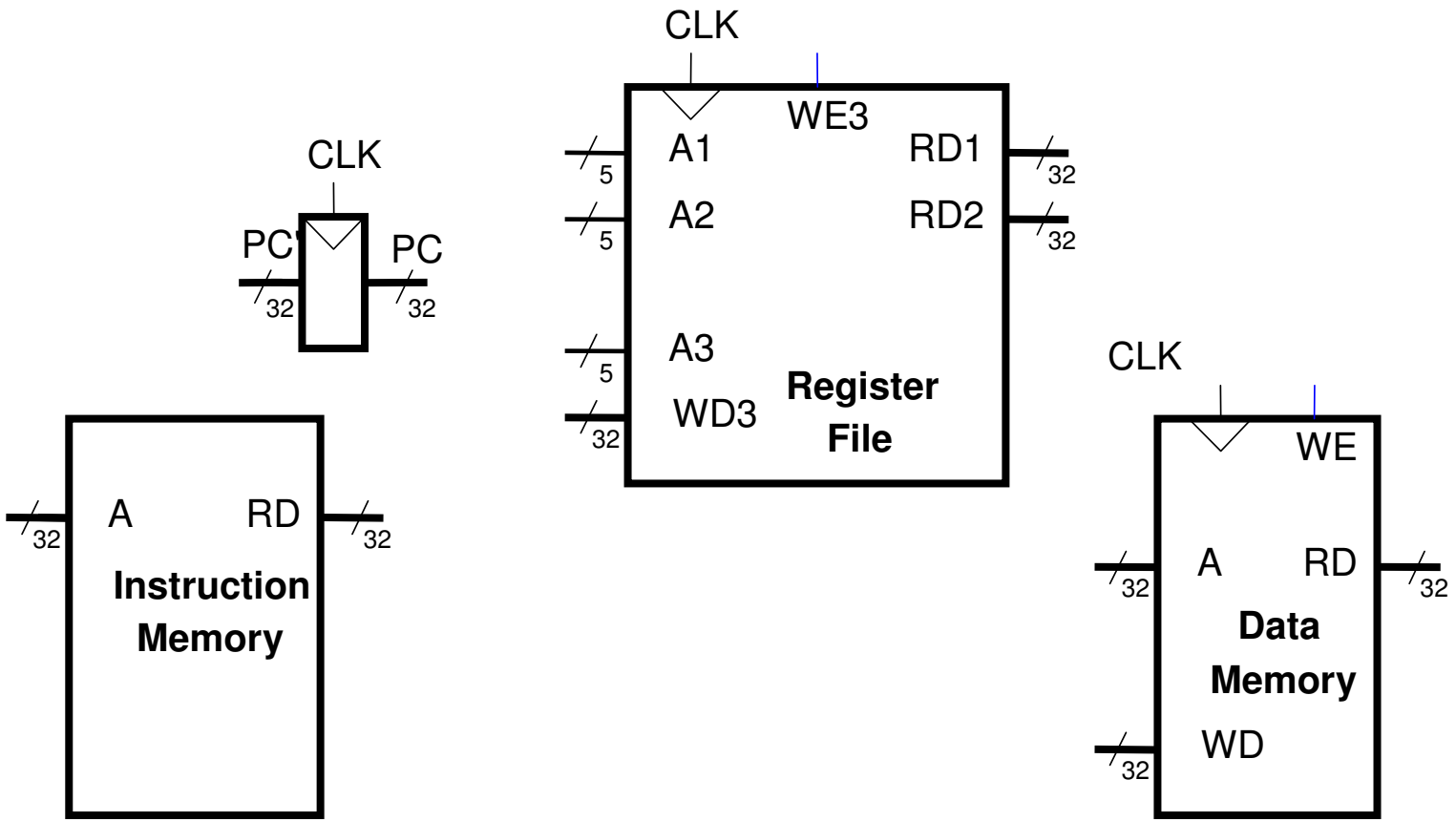


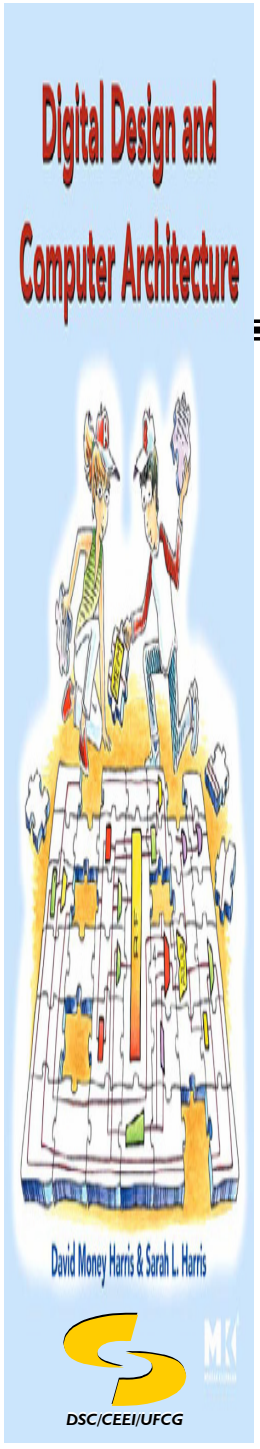
Micro-Arquitetura

- Estado da Arquitetura
  - Determina o estado do Processador em um dado instante de tempo
    - **PC**
    - **32 registradores**
    - **Memória**

Microarquitetura

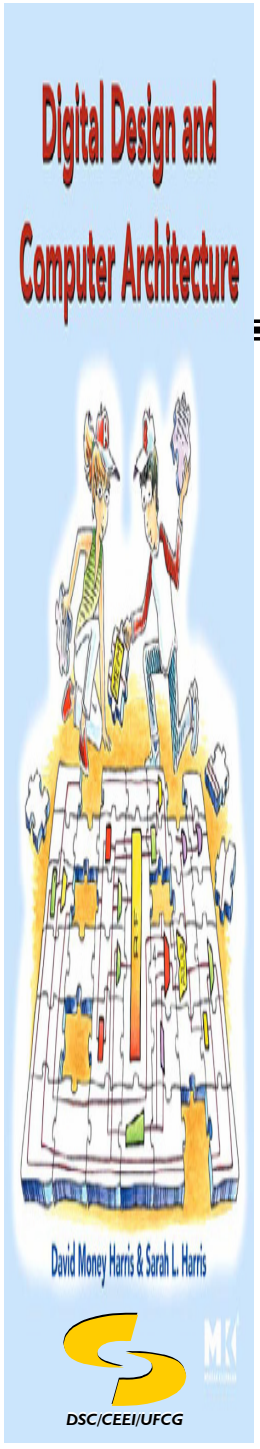
- Elementos de estados do MIPS:





Microarquitetura - Processador MIPS

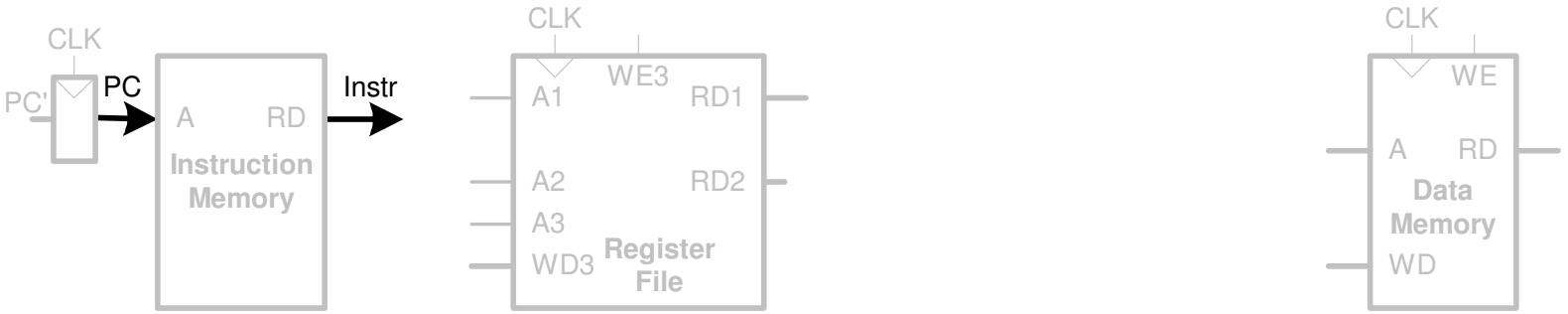
- *Datapath*
- Unidade de Controle

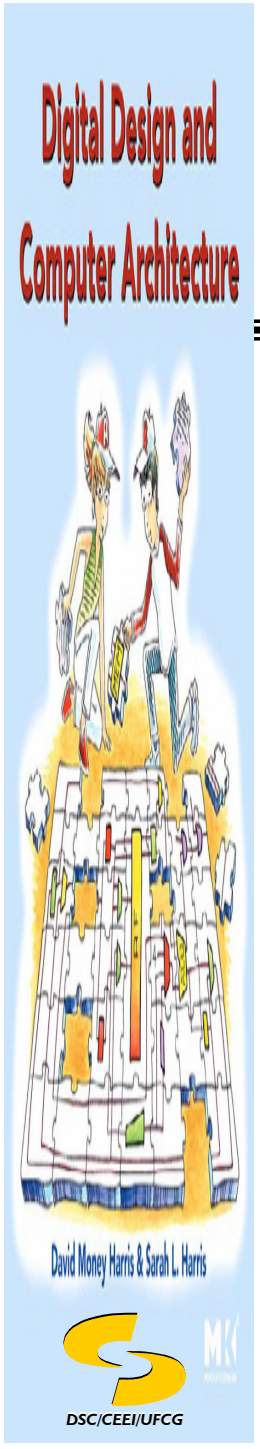


Processador MIPS Single-Cycle

- **Execução de `lw`**

1: Fetch da Instrução

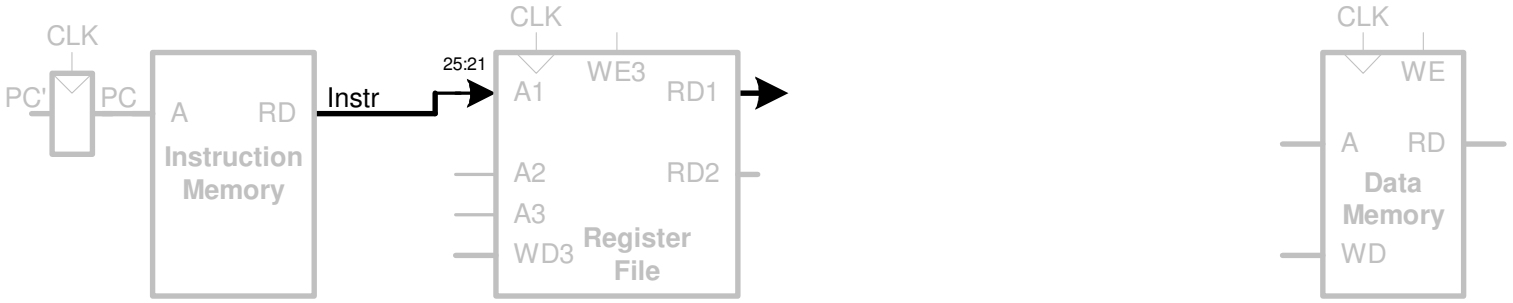


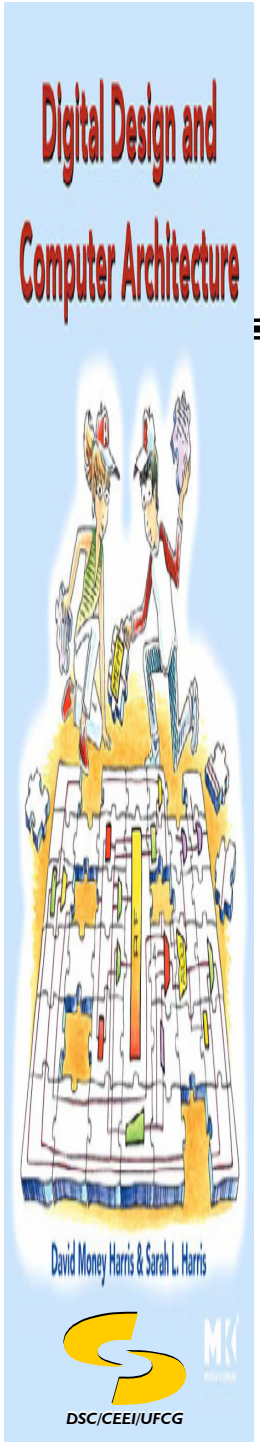


Processador MIPS Single-Cycle

- **Execução de `lw`**

2: Lê o operando fonte do RF

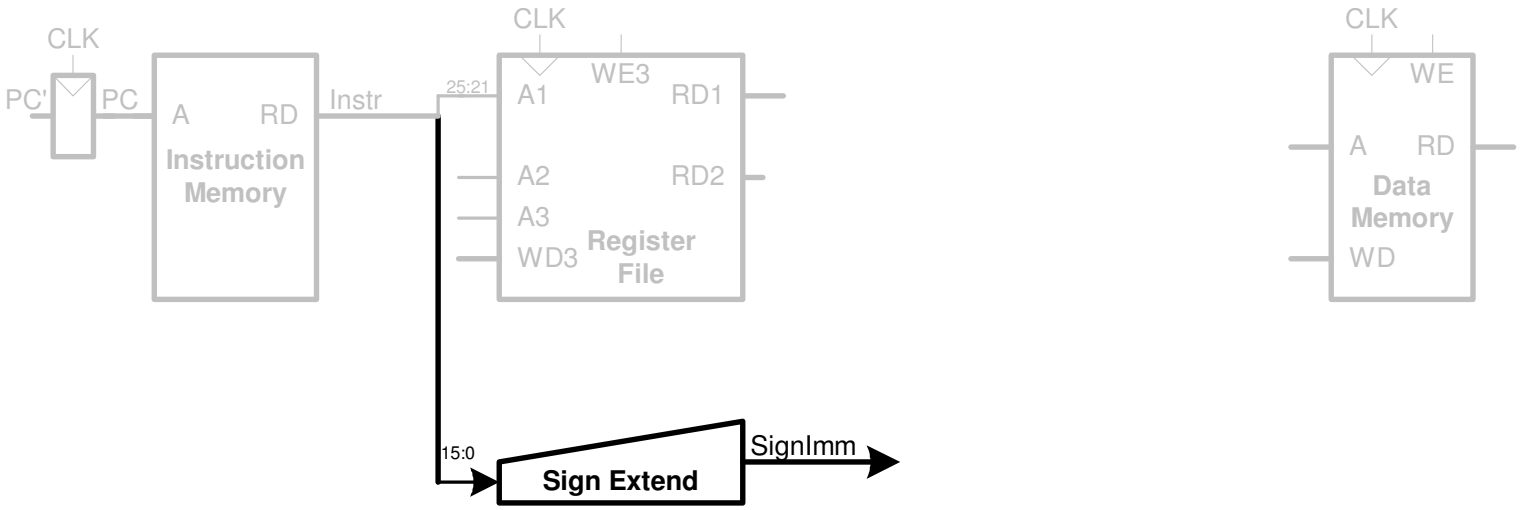


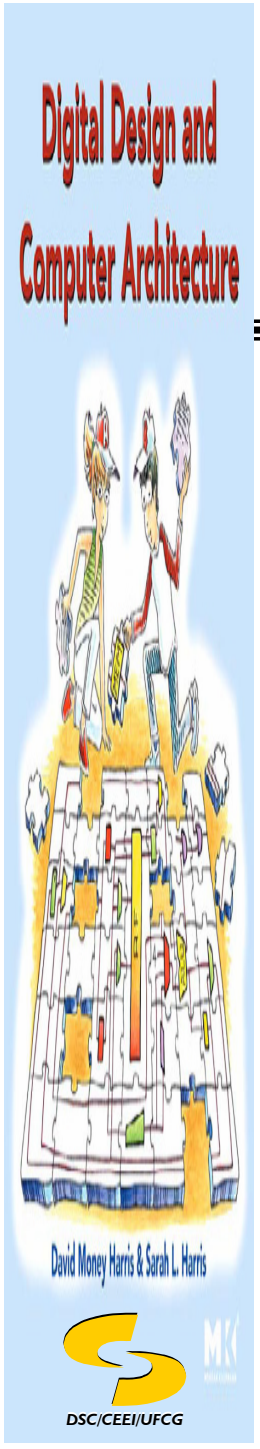


Processador MIPS Single-Cycle

- **Execução de `lw`**

3: Sign-extend o imediato

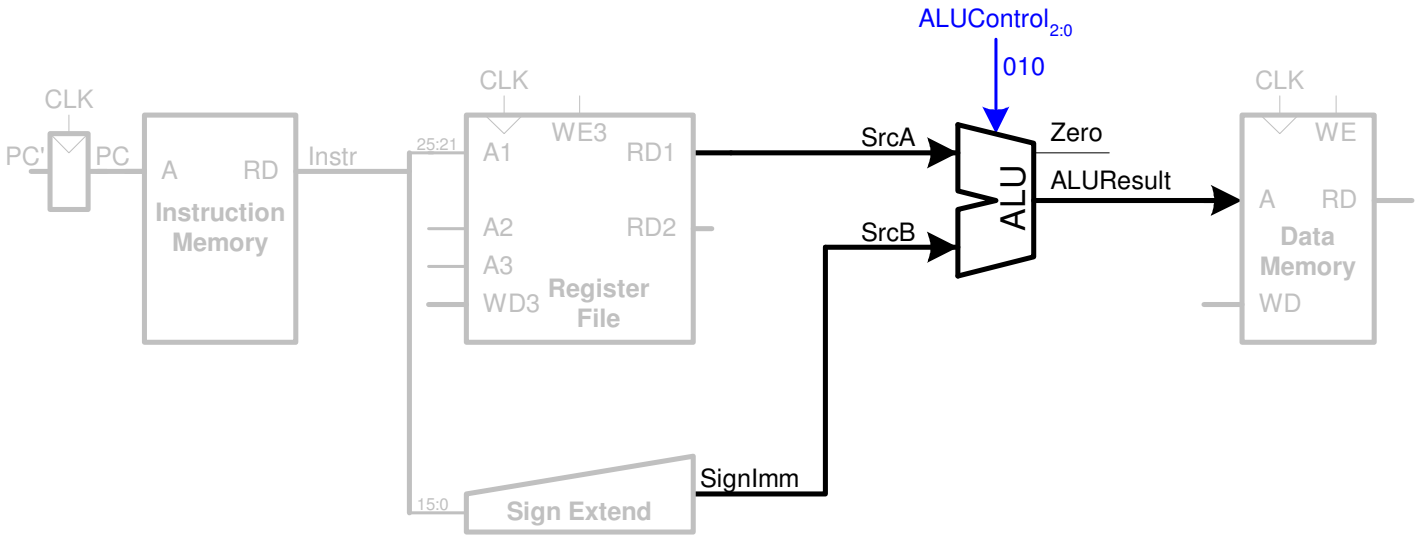


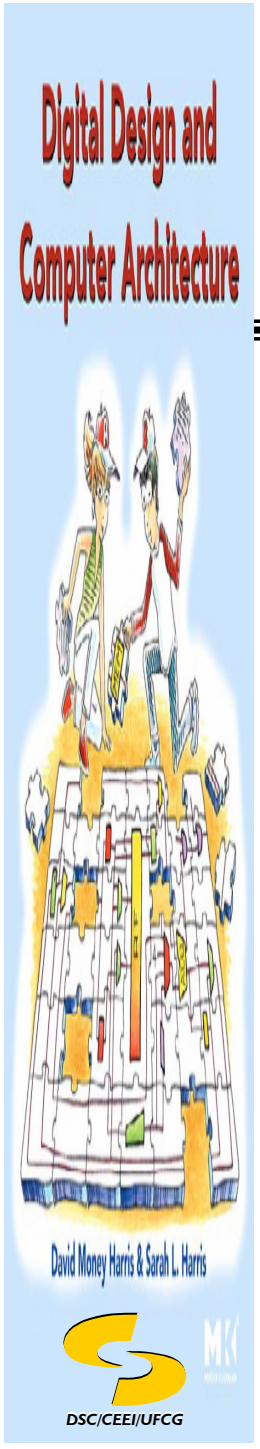


Processador MIPS Single-Cycle

- **Execução de `lw`**

4: Calcula o endereço efetivo de memória

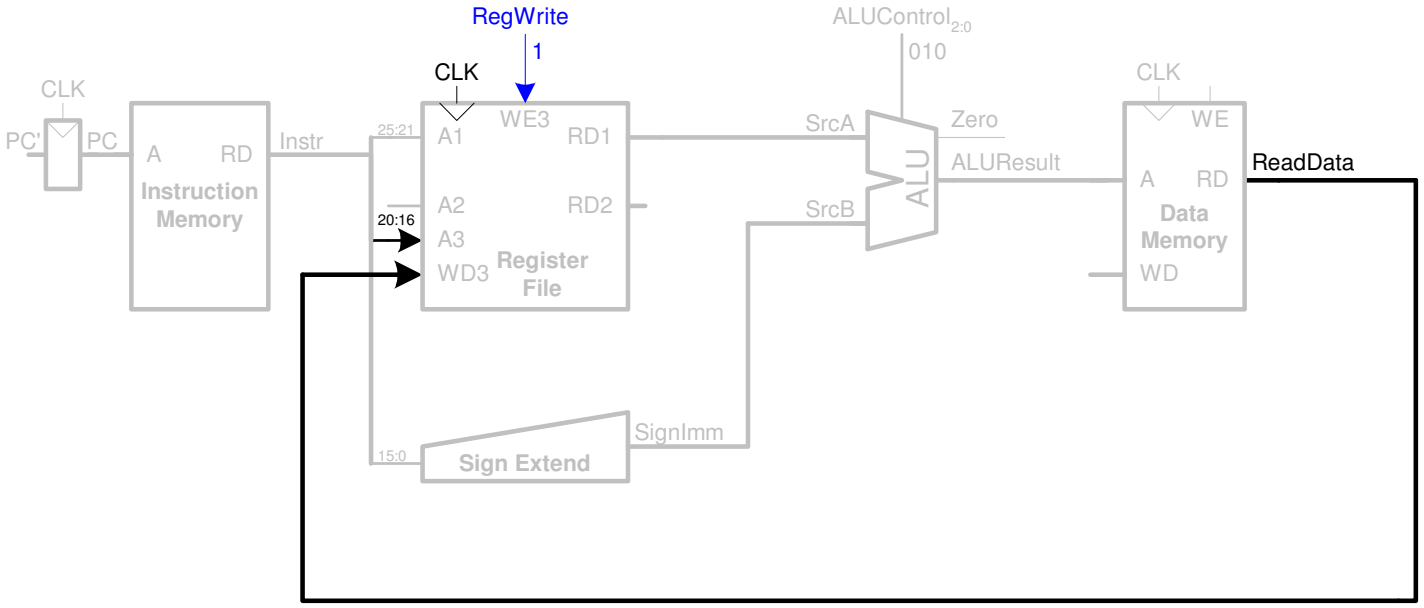


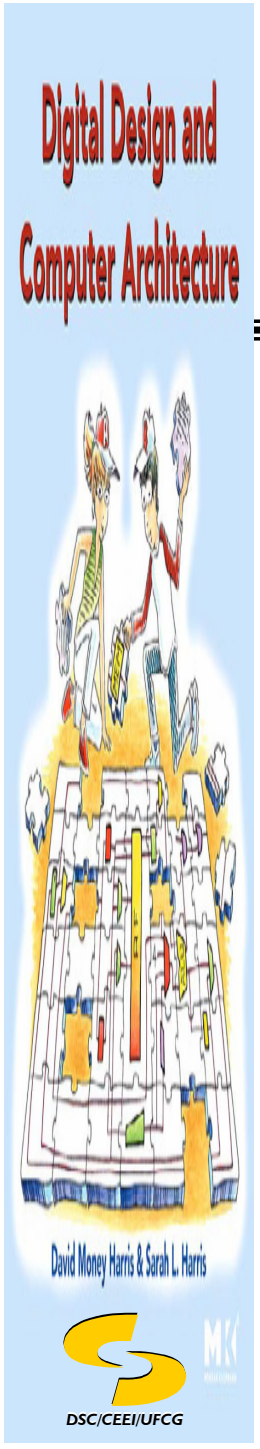


Processador MIPS Single-Cycle

- **Execução de `lw`**

5: Lê o dado da memória e o escreva no RF

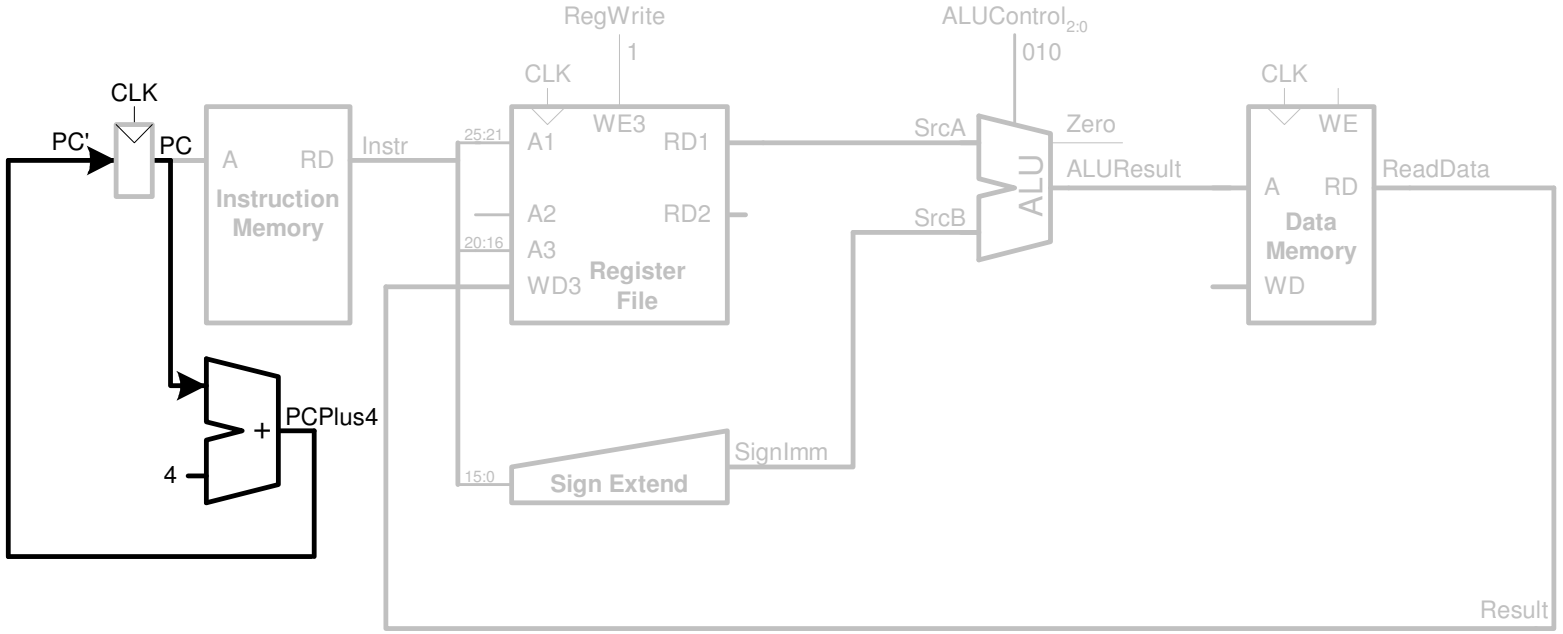


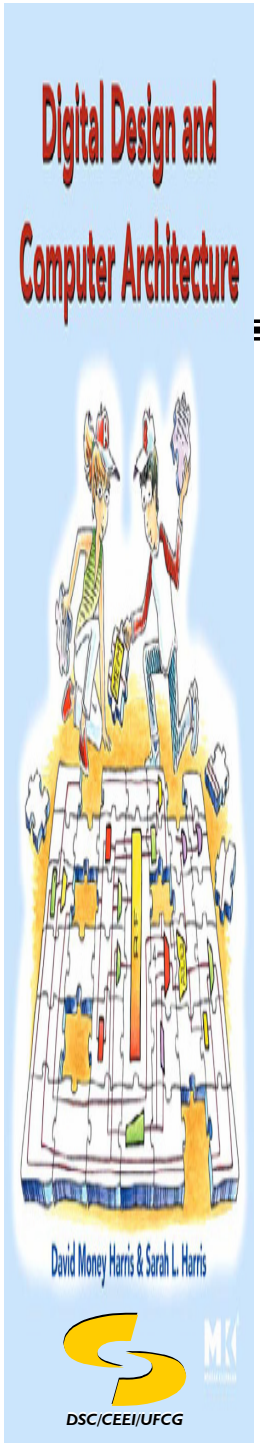


Processador MIPS Single-Cycle

- **Execução de `lw`**

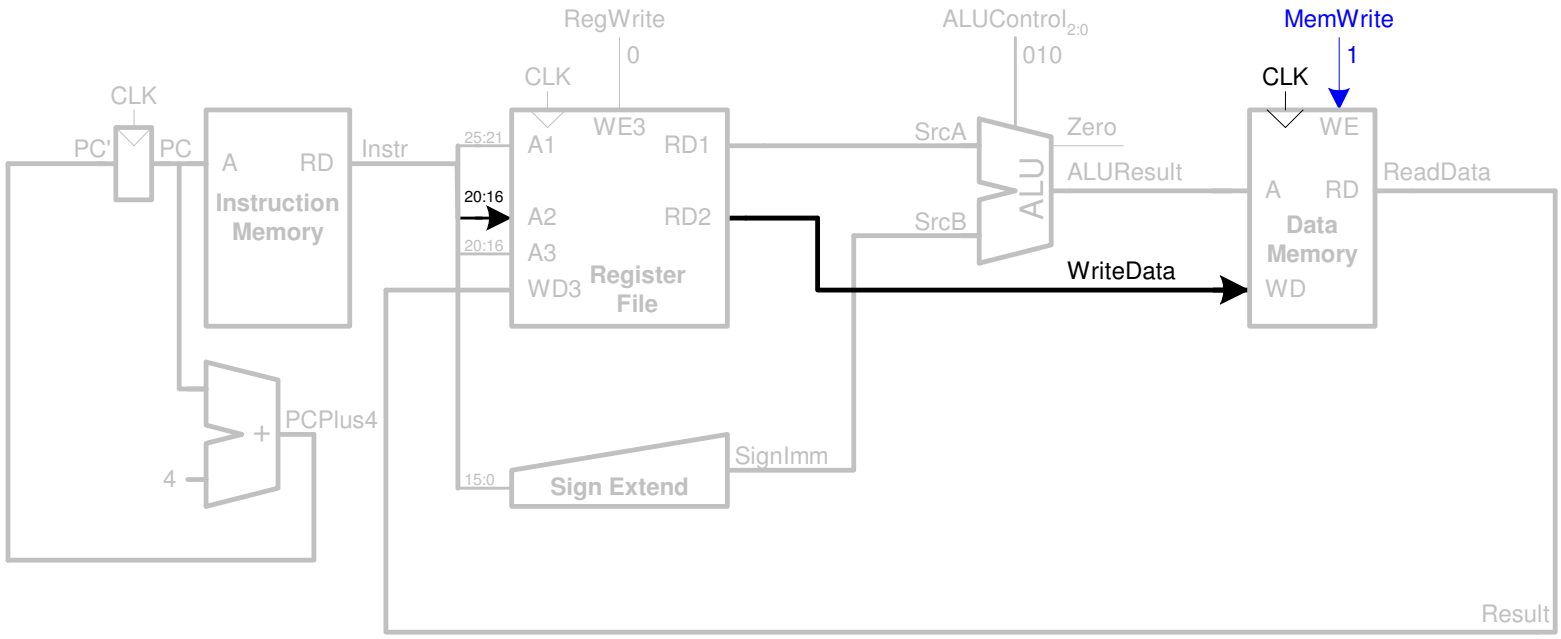
6: Determina o endereço da próxima instrução

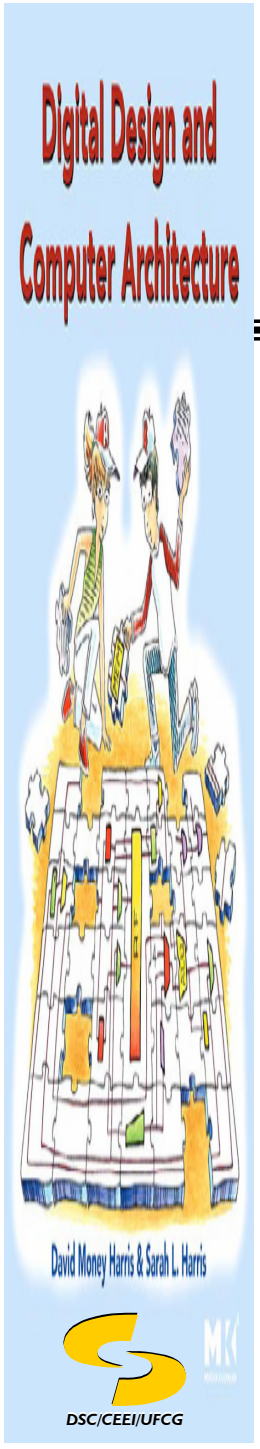




Processador MIPS Single-Cycle

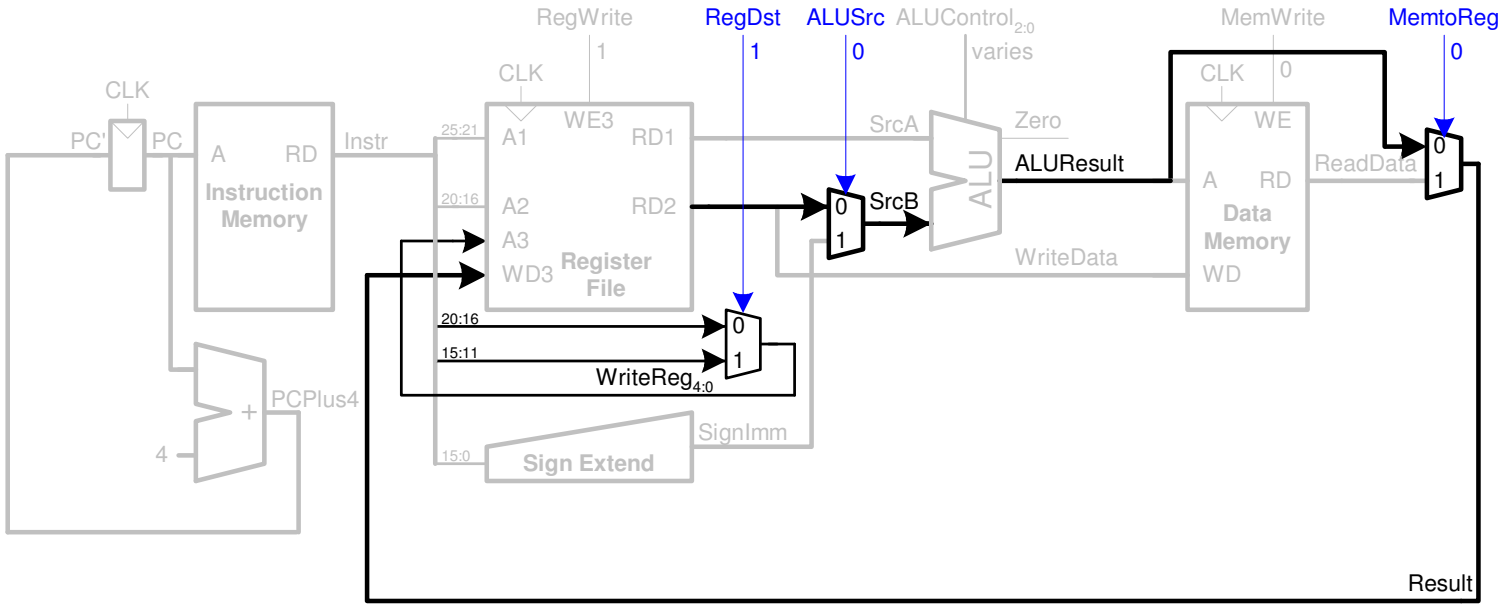
- **Execução de `sw`**
  - Precisa escrever o valor do registrador na memória

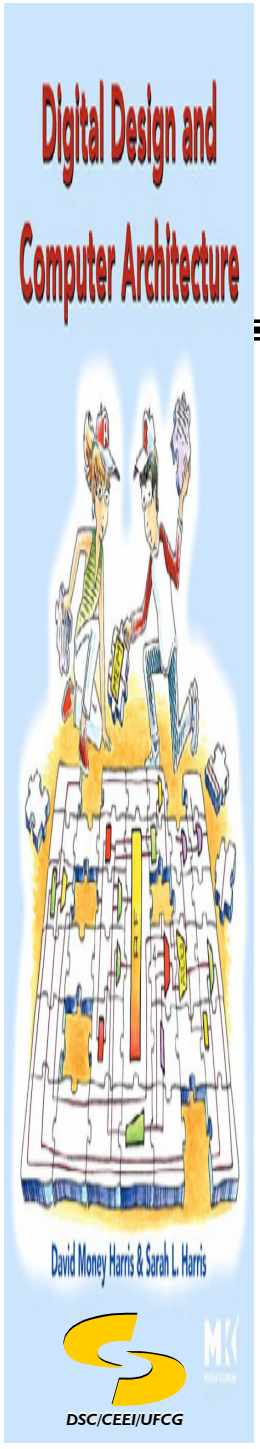




Processador MIPS Single-Cycle

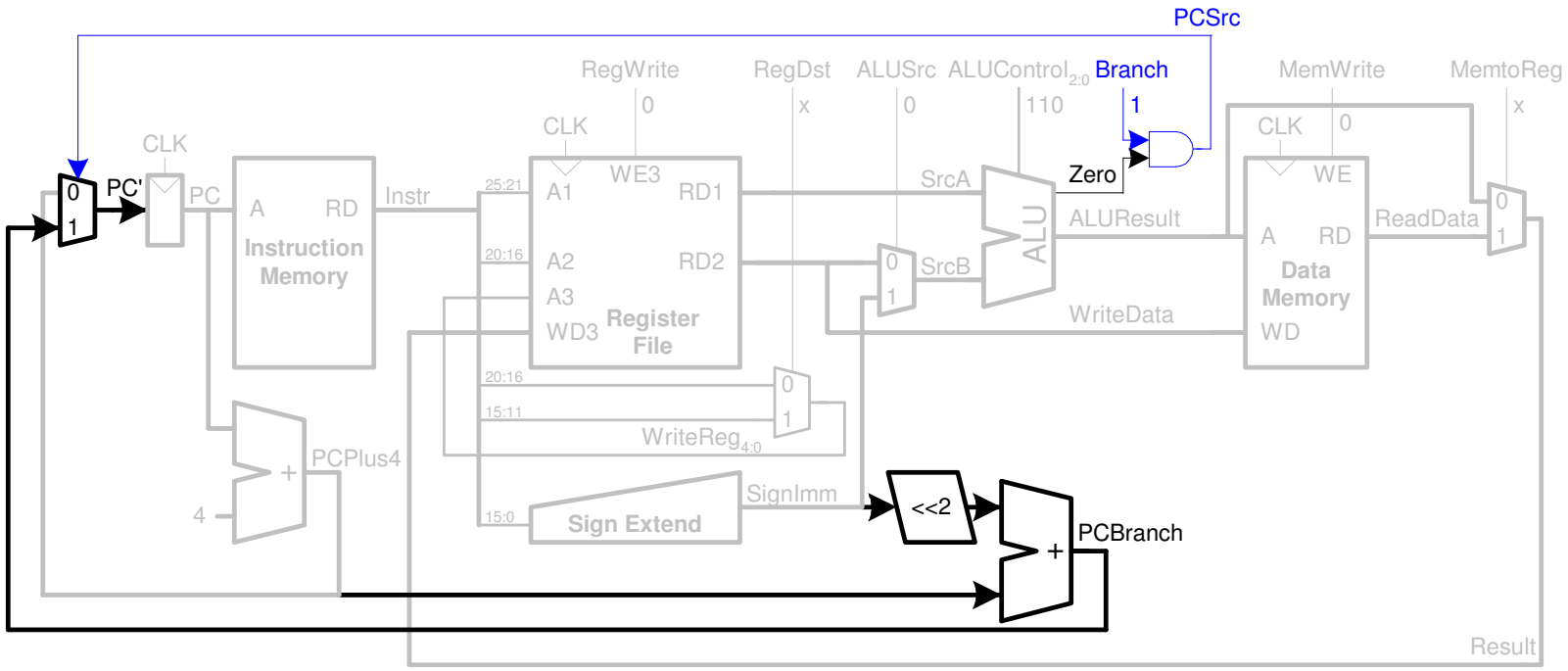
- **Instruções R-Type**: `add, sub, and, or, ….`
  - Escrever *ALUResult no RF*
    - Escreve em `rd` e não em `rt`

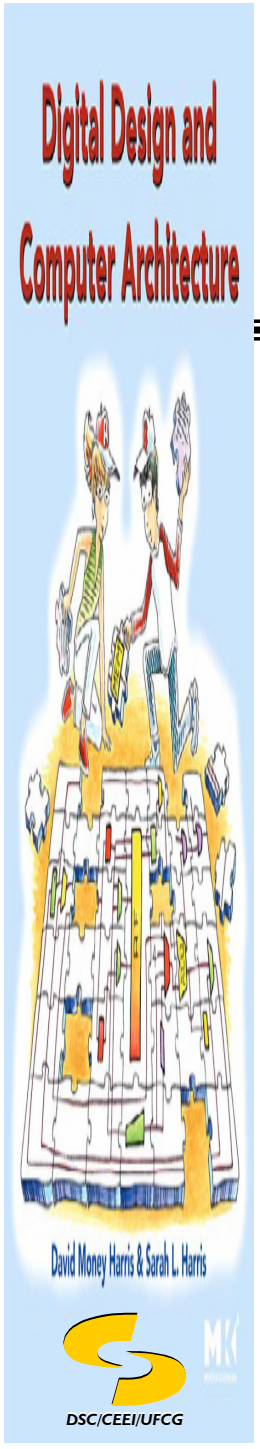




Processador MIPS Single-Cycle

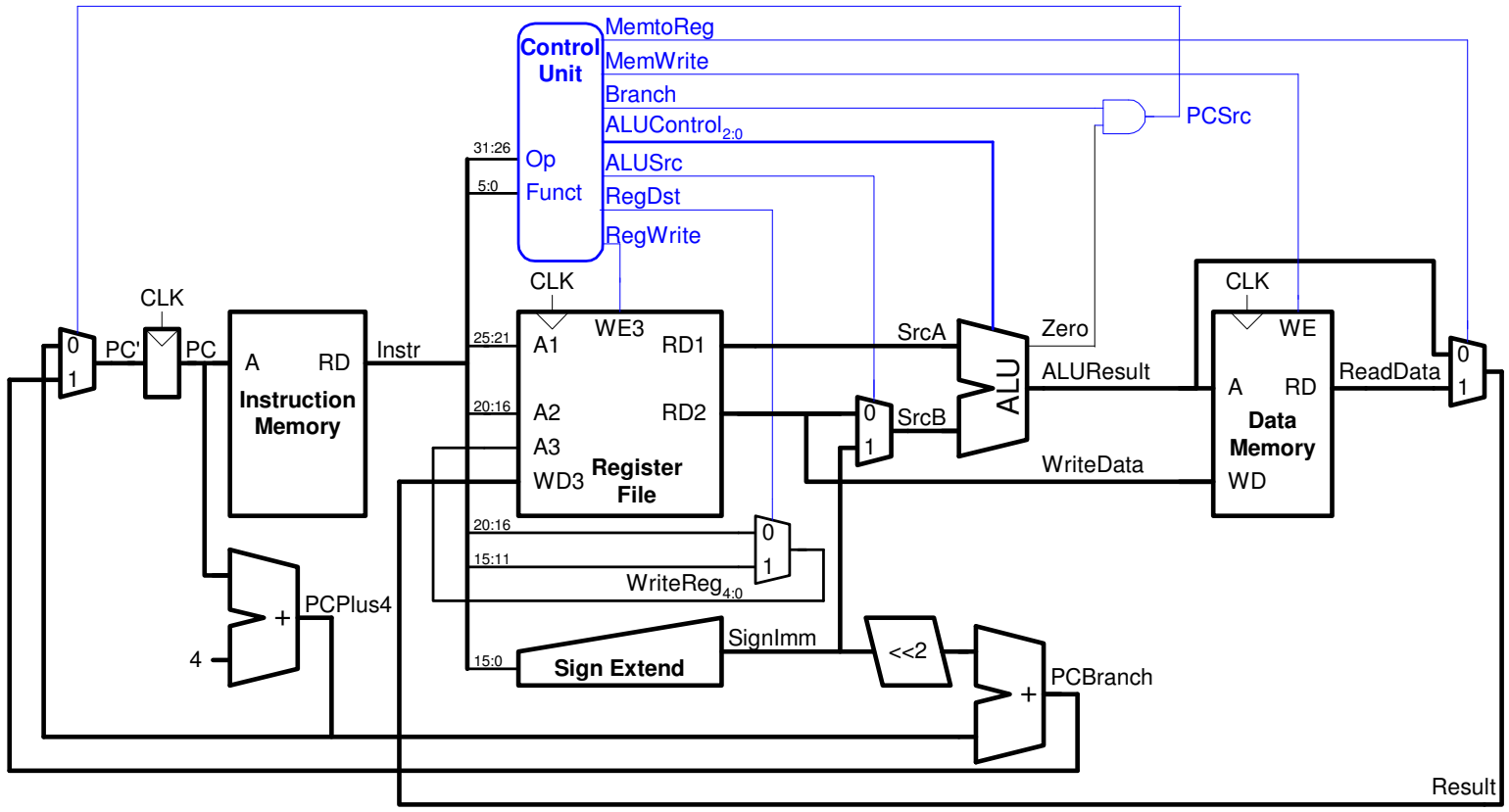
- **Instrução `beq`**
  - Determina se os conteúdos dos registradores são iguais
  - Calcula o endereço alvo do desvio
    - (sign-extended immediate + PC+4)

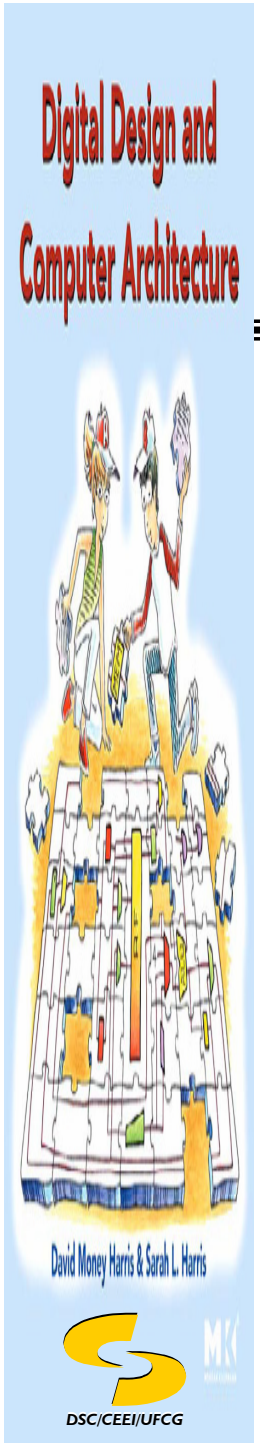




Processador MIPS Single-Cycle

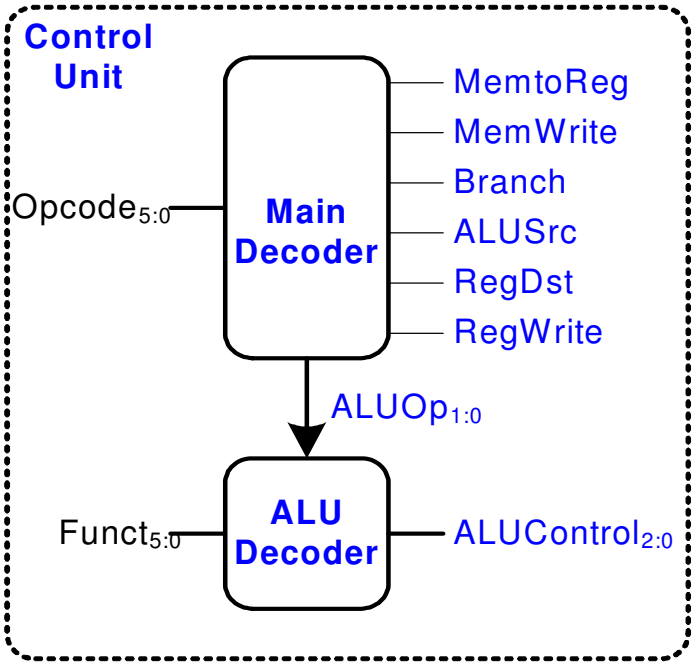
Unidade de Controle

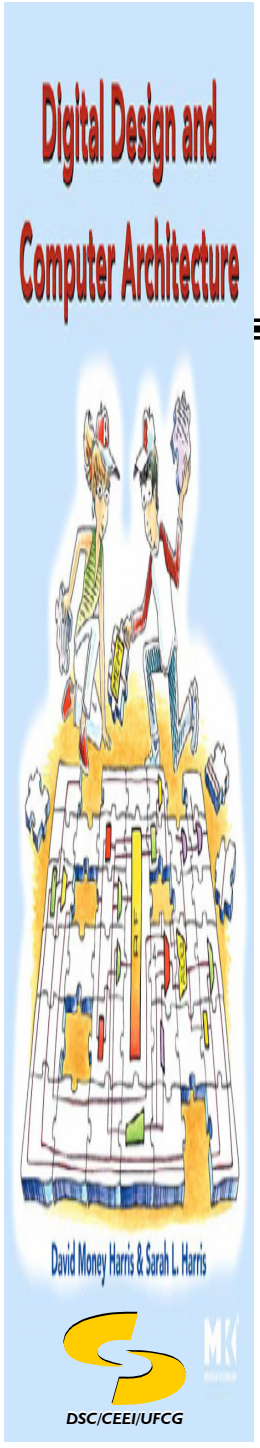




Processador MIPS Single-Cycle

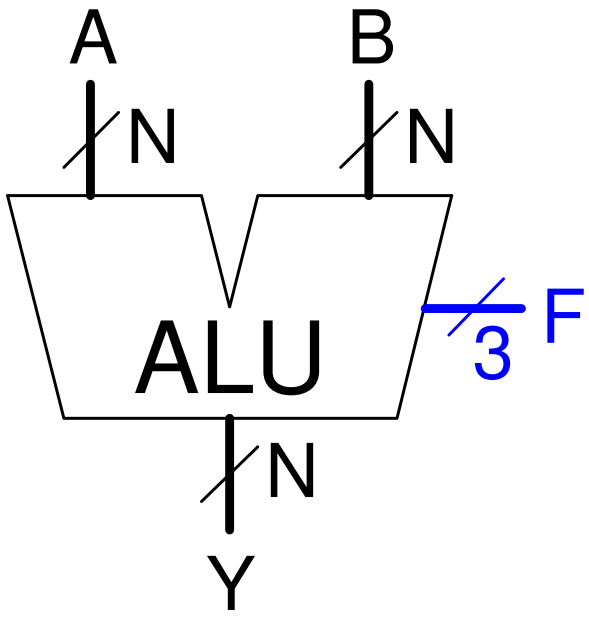
Control Unit



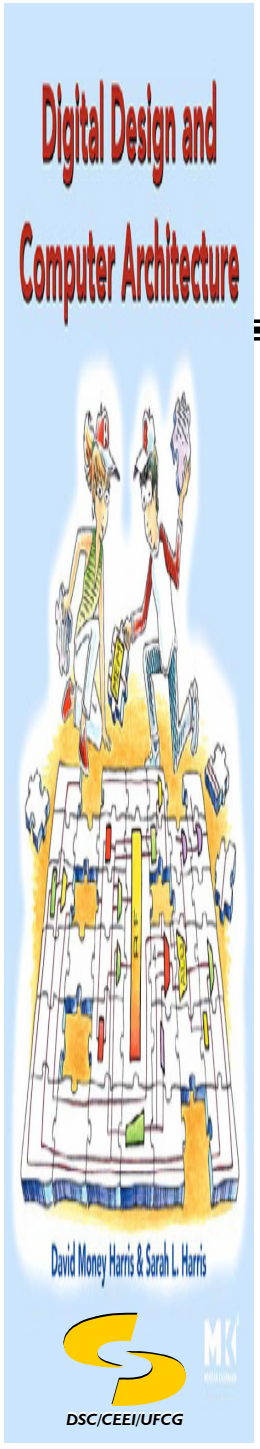


Processador MIPS Single-Cycle

ALU

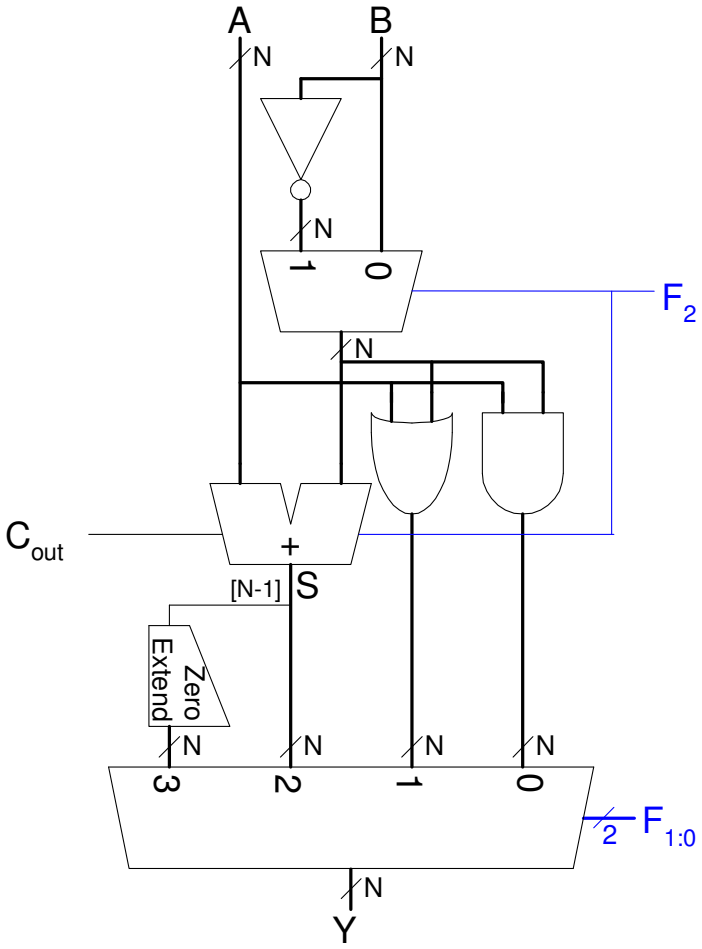


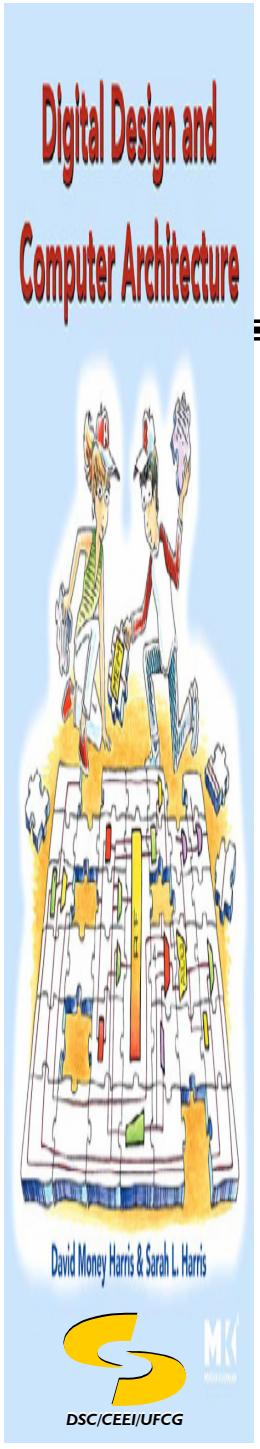
$F_{2:0}$	Function
000	A & B
001	A | B
010	A + B
011	not used
100	A & ~B
101	A | ~B
110	A - B
111	SLT



Processador MIPS Single-Cycle

ALU



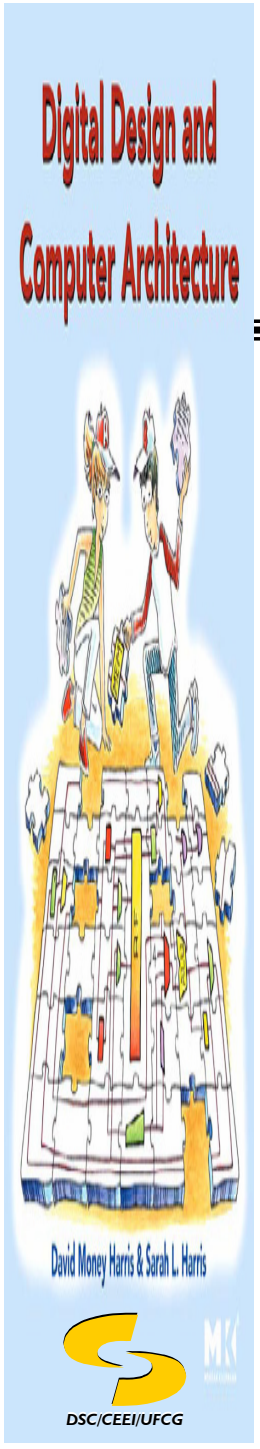


Processador MIPS Single-Cycle

ALU Decoder

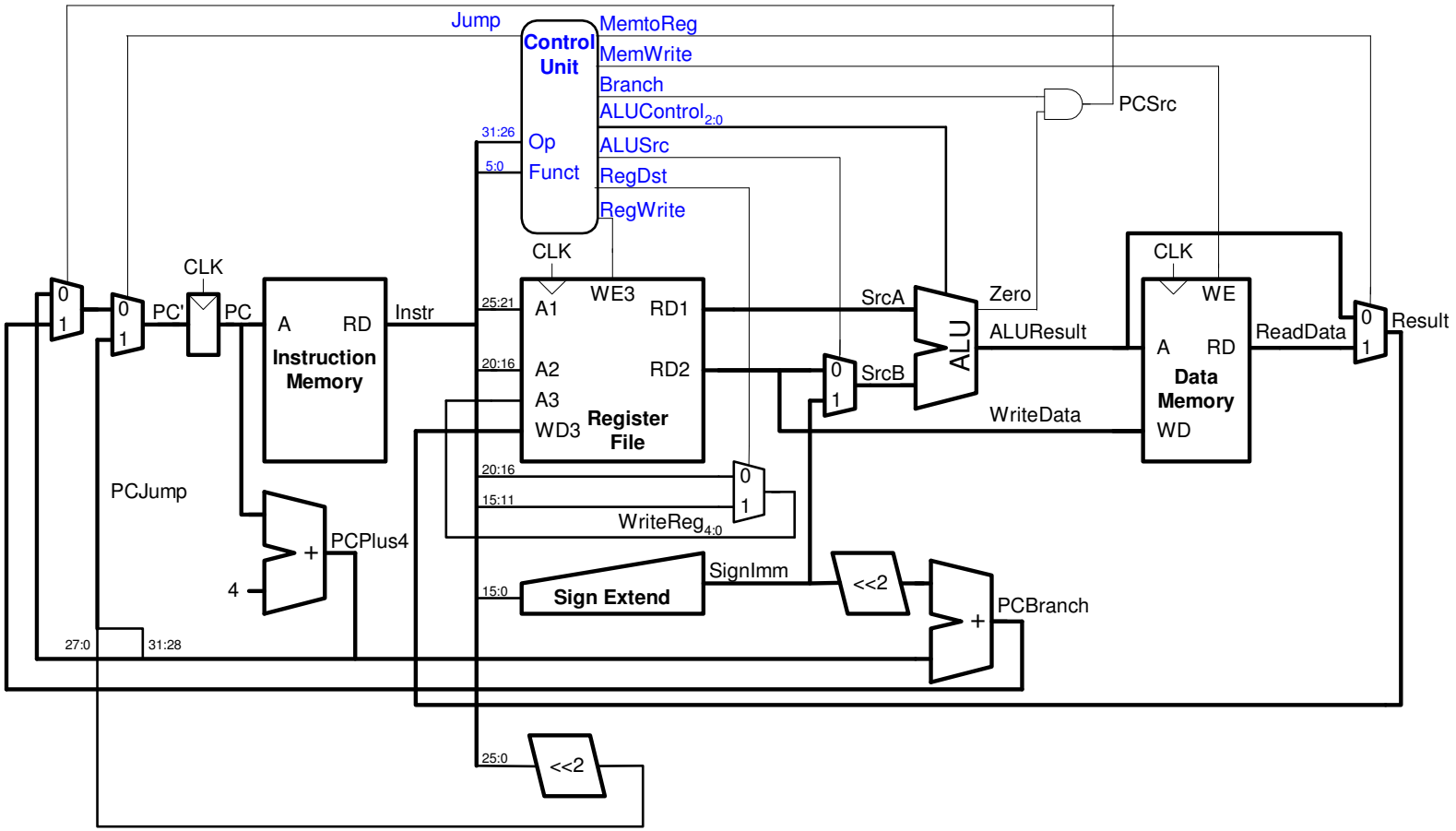
$ALUOp_{1:0}$	Meaning
00	Add
01	Subtract
10	Look at Funct
11	Not Used

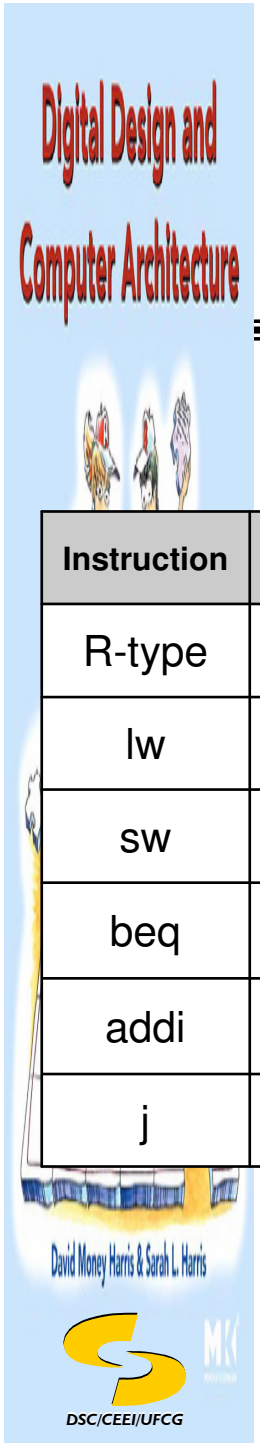
$ALUOp_{1:0}$	Funct	$ALUControl_{2:0}$
00	X	010 (Add)
X1	X	110 (Subtract)
1X	100000 (`add`)	010 (Add)
1X	100010 (`sub`)	110 (Subtract)
1X	100100 (`and`)	000 (And)
1X	100101 (`or`)	001 (Or)
1X	101010 (`slt`)	111 (SLT)



Processador MIPS Single-Cycle

- Funcionalidades

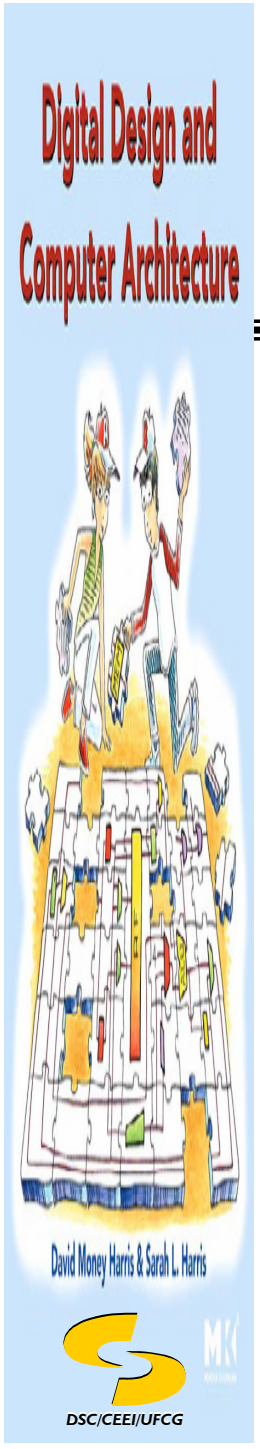




Processador MIPS Single-Cycle

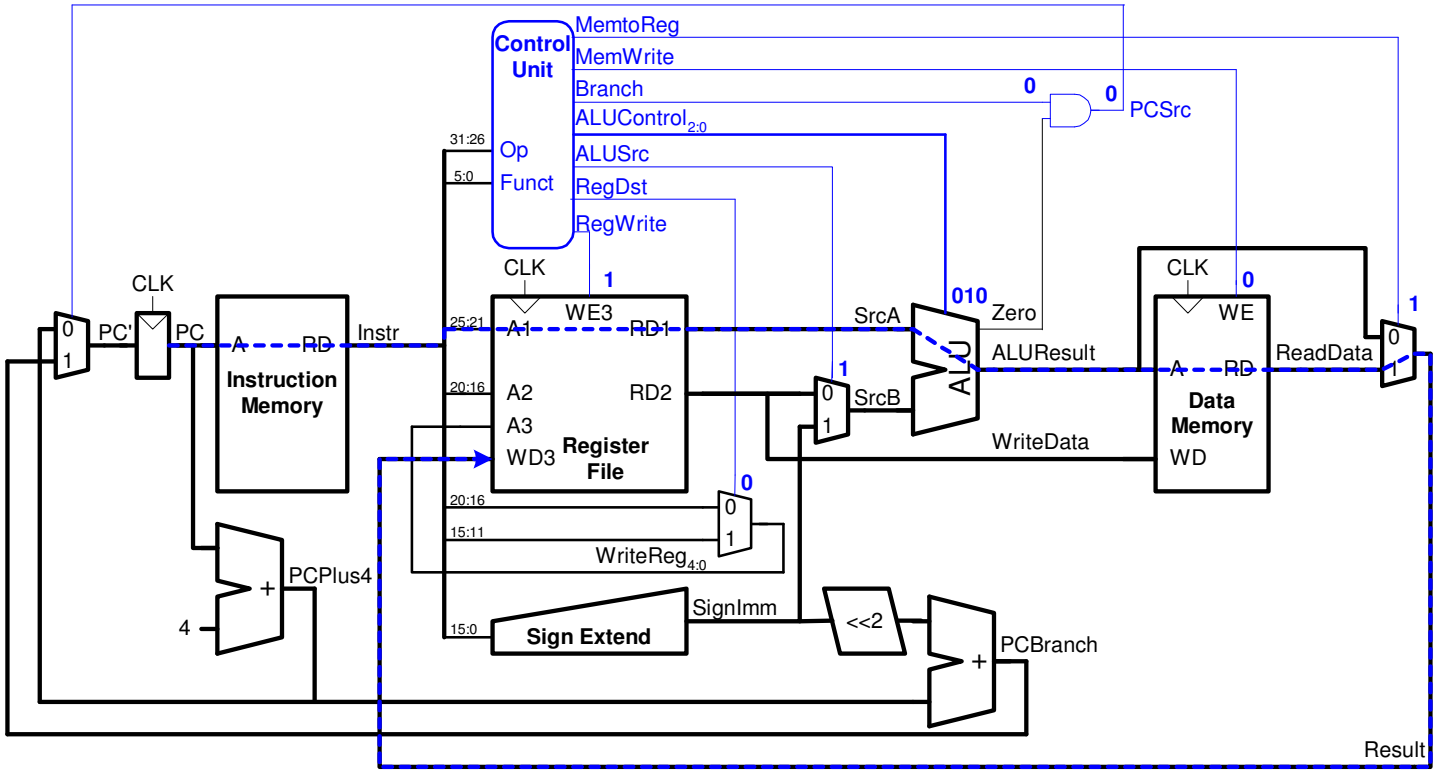
- Decodificador Principal

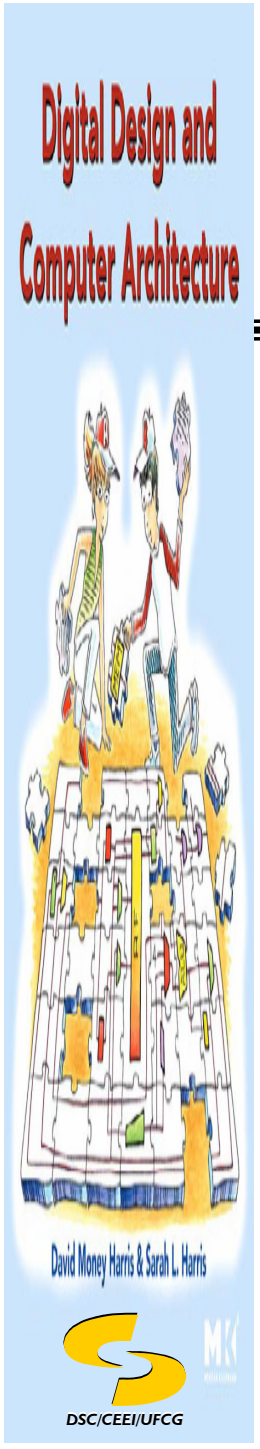
Instruction	$Op_{5:0}$	RegWrite	RegDst	AluSrc	Branch	MemWrite	MemtoReg	$ALUOp_{1:0}$	Jump
R-type	000000	1	1	0	0	0	0	10	0
lw	100011	1	0	1	0	0	1	00	0
sw	101011	0	X	1	0	1	X	00	0
beq	000100	0	X	0	1	0	X	01	0
addi	001000	1	0	1	0	0	0	00	0
j	000100	0	X	X	X	0	X	XX	1



Processador MIPS Single-Cycle

- Desempenho: Quão rápido é o processador?
- `Cycle time`: limitado pelo caminho crítico - `lw`





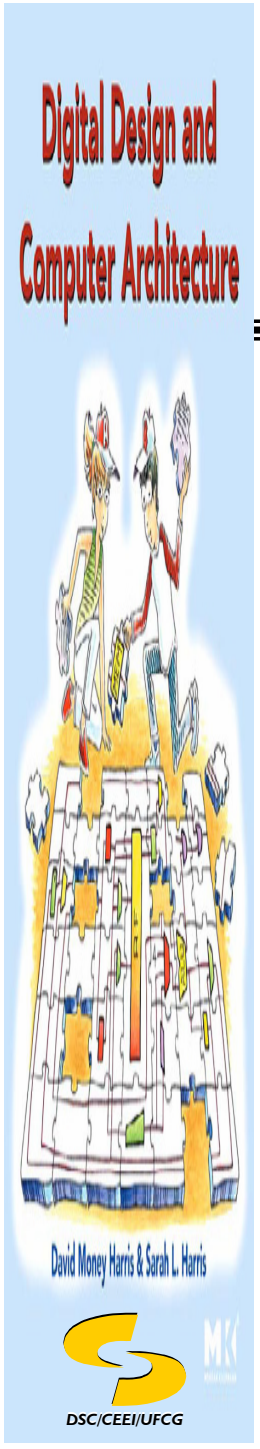
Processador MIPS Single-Cycle

- **Caminho crítico**

$$T_c = t_{pcq\_PC} + t_{mem} + \max(t_{RFread}, t_{sext}) + t_{mux} + t_{ALU} + t_{mem} + t_{mux} + t_{RFsetup}$$

- Na maioria das implementações os caminhos limitantes são: memória, ALU, register file. Assim,

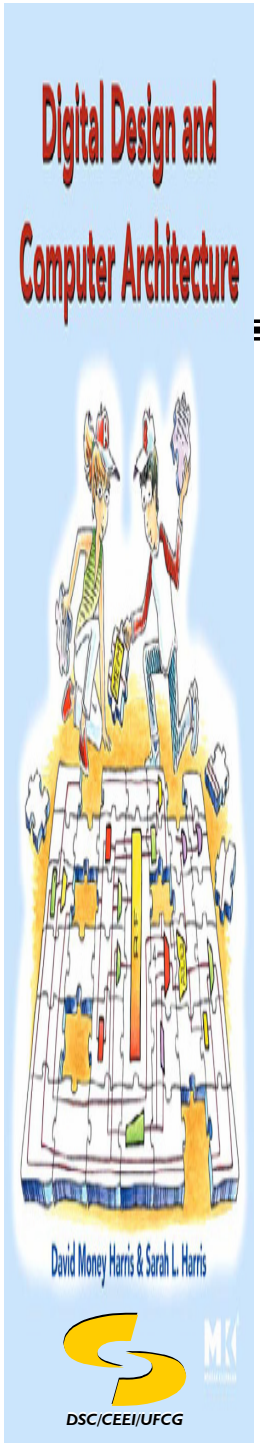
$$T_c = t_{pcq\_PC} + 2t_{mem} + t_{RFread} + 2t_{mux} + t_{ALU} + t_{RFsetup}$$



Processador MIPS Single-Cycle

Element	Parameter	Delay (ps)
Register clock-to-Q	t_{pcq_PC}	30
Register setup	t_{setup}	20
Multiplexer	t_{mux}	25
ALU	t_{ALU}	200
Memory read	t_{mem}	250
Register file read	t_{RFread}	150
Register file setup	$t_{RFsetup}$	20

$$T_c = t_{pcq\_PC} + 2t_{mem} + t_{RFread} + 2t_{mux} + t_{ALU} + t_{RFsetup}$$
$$= [30 + 2(250) + 150 + 2(25) + 200 + 20] \text{ ps}$$
$$= 950 \text{ ps}$$



Processador MIPS Single-Cycle

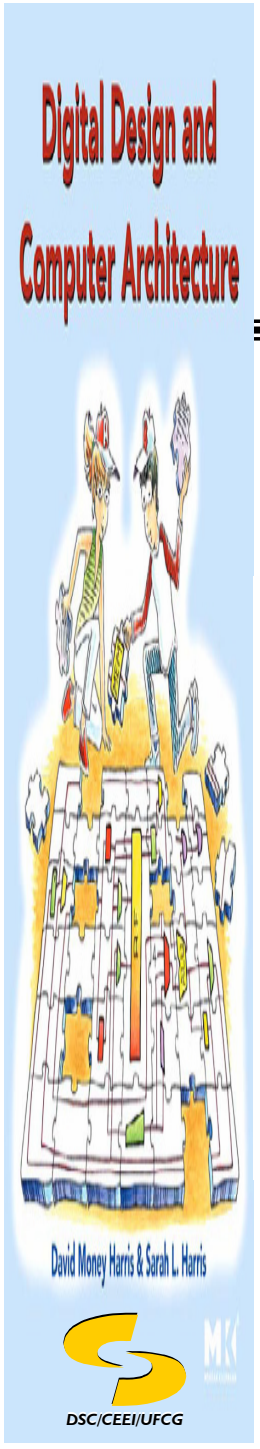
- Para um programa com 100 bilhões de instruções executando em um processador MIPS single-cycle,

- ***Execution Time***

  = (# *instructions*)(*cycles/instruction*)(*seconds/cycle*)

  = $(100 \times 10^9)(1)(950 \times 10^{-12}\ \text{s})$

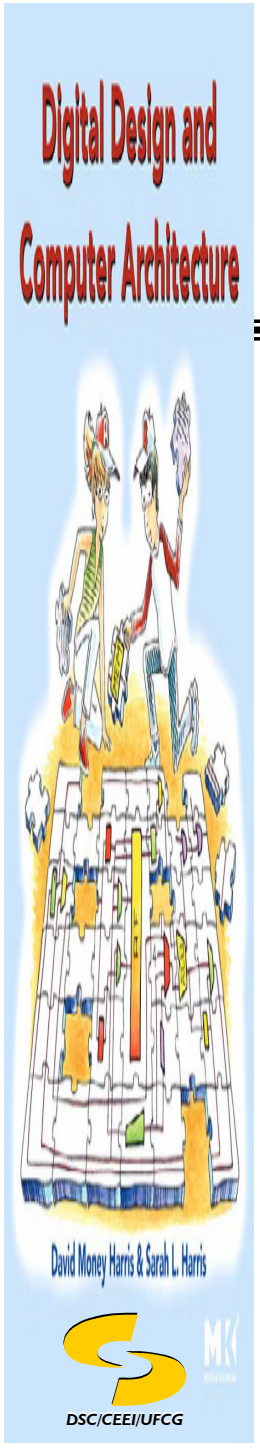
  = 95 *seconds*



Processadores Intel

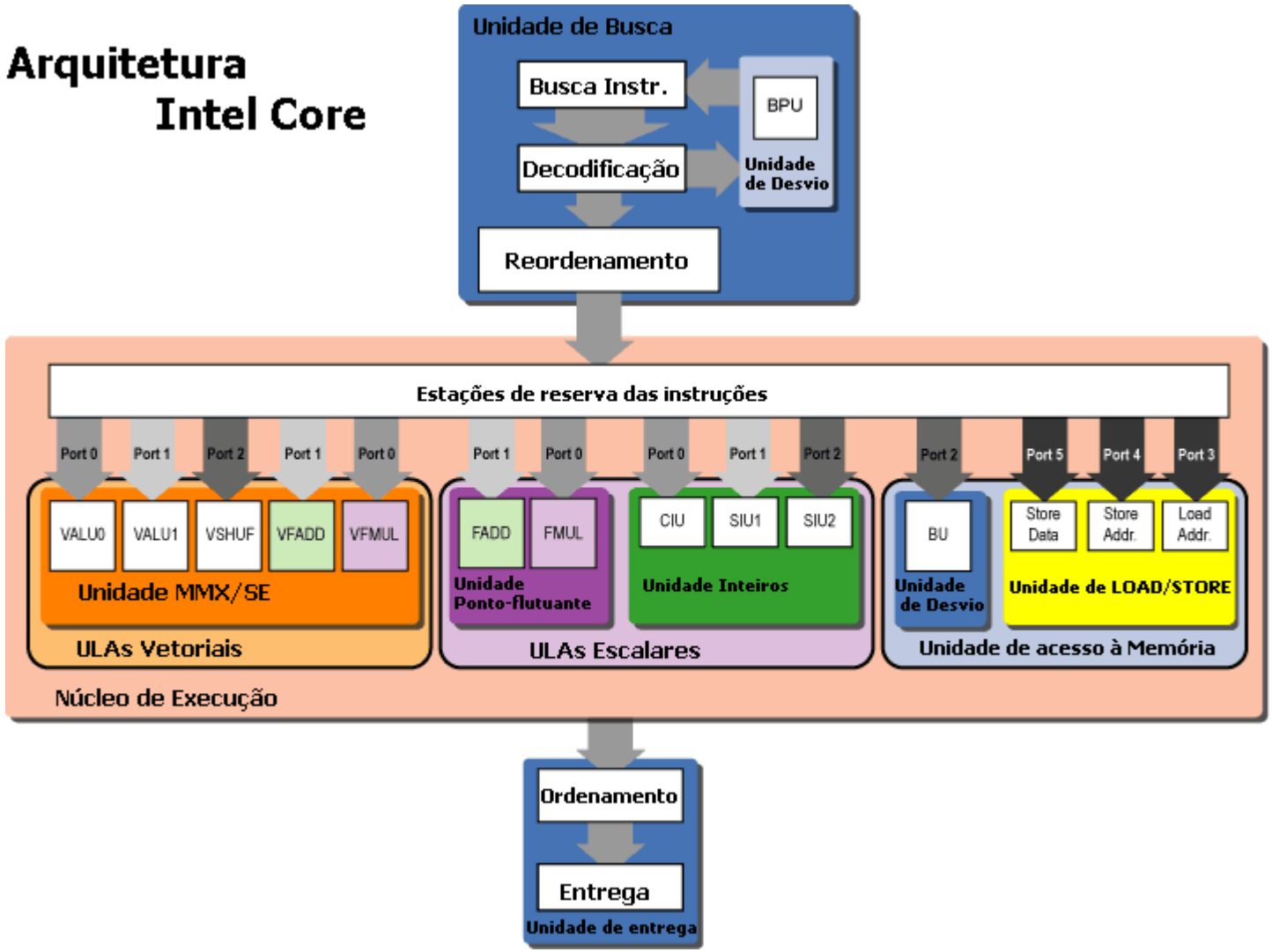
Evolução dos Microprocessadores Intel

Processor	Year	Feature Size (μm)	Transistors	Frequency (MHz)	Microarchitecture
80386	1985	1.5–1.0	275k	16–25	multicycle
80486	1989	1.0–0.6	1.2M	25–100	pipelined
Pentium	1993	0.8–0.35	3.2–4.5M	60–300	superscalar
Pentium II	1997	0.35–0.25	7.5M	233–450	out of order
Pentium III	1999	0.25–0.18	9.5M–28M	450–1400	out of order
Pentium 4	2001	0.18–0.09	42–178M	1400–3730	out of order
Pentium M	2003	0.13–0.09	77–140M	900–2130	out of order
Core Duo	2005	0.065	152M	1500–2160	dual core



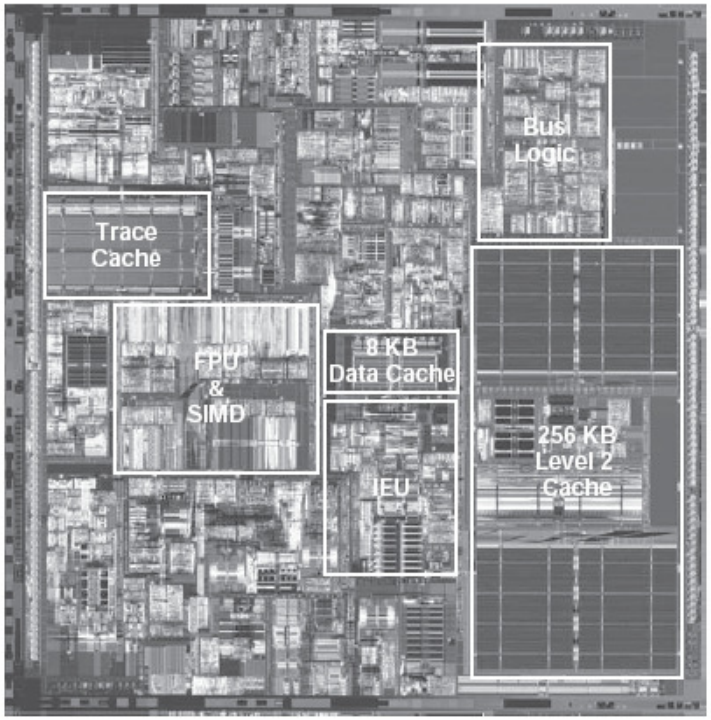
Processadores Intel

Arquitetura Intel Core

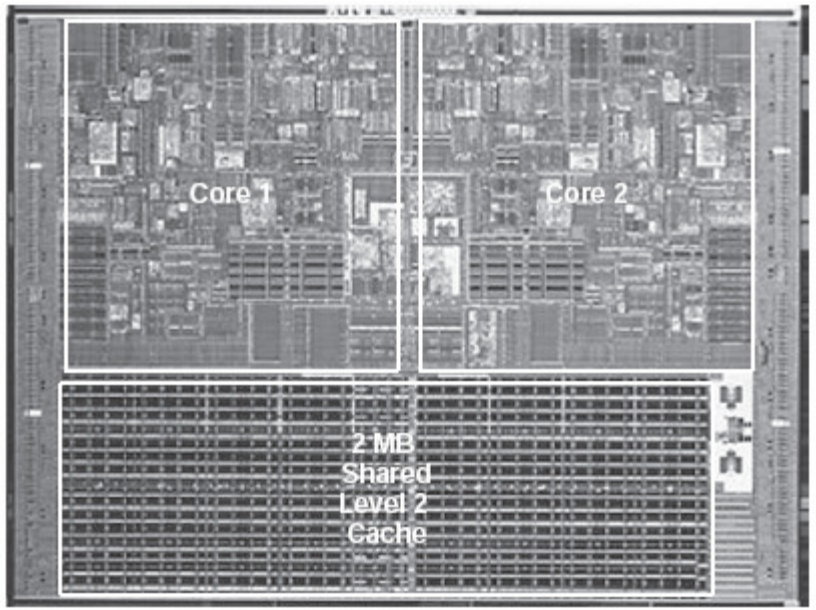


Processadores Intel IA-32

Chip do Pentium 4

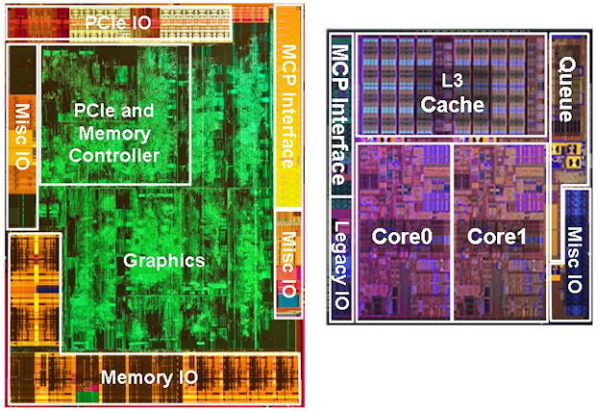


Chip do Core Duo

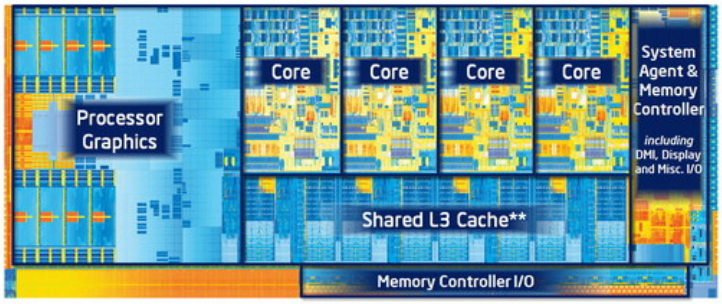


Processadores Intel IA-32

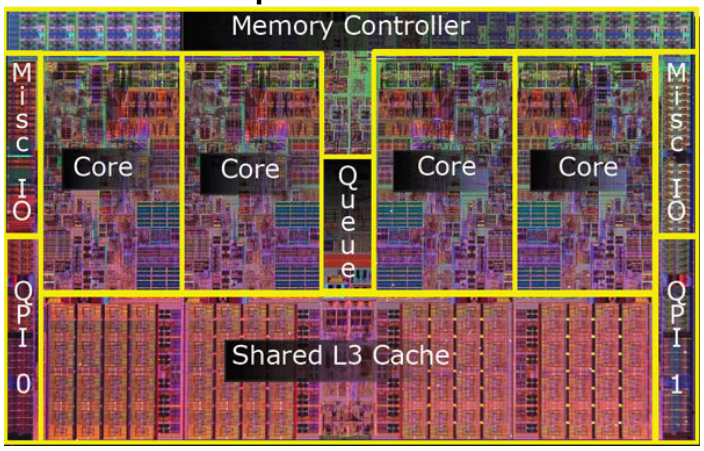
Chip do Core i3

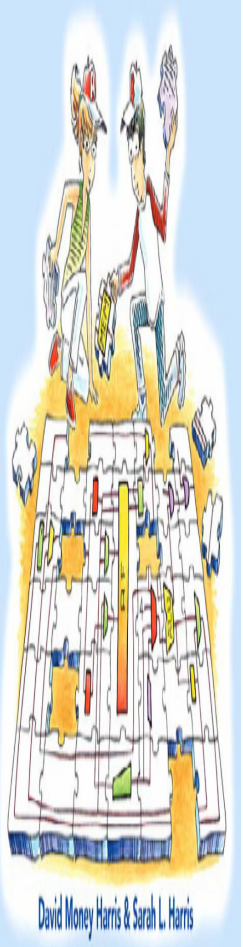


Chip do Core i5



Chip do Core i7





Processadores Intel IA-32

Code name	Key products	Cores	Threads	Last-level cache size	Process node (Nanometers)	Estimated transistors (Millions)	Die area (mm^2)
Penryn	Core 2 Duo	2	2	6 MB	45	410	107
Bloomfield	Core i7	4	8	8 MB	45	731	263
Lynnfield	Core i5, i7	4	8	8 MB	45	774	296
Westmere	Core i3, i5	2	4	4 MB	32	383	81
Deneb	Phenom II	4	4	6 MB	45	758	258
Propus	Athlon II	4	4	512 KB x 4	45	300	169

Fonte: http://techreport.com/review/18216/intel-core-i3-and-i5-dual-core-processors